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DERWENT-ACC-NO: 2005-138527

DERWENT-WEEK: 200515

TITLE: Chip stack package

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PATENT-ASSIGNEE: HYNIX SEMICONDUCTOR INC[HYNIN]

PRIORITY-DATA: 2003KR-0019996 (March 31, 2003)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
KR 2004085348 A	October 8, 2004	N/A	001	H01L 023/12

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
KR2004085348A	N/A	2003KR-0019996	March 31, 2003

INT-CL (IPC): H01L023/12

ABSTRACTED-PUB-NO: KR2004085348A

BASIC-ABSTRACT:

NOVELTY - A chip stack package is provided to easily fabricate and to prevent molding defect and warpage of a bonding wire by using a substrate with a window for exposing a groove and a bonding pad.

DETAILED DESCRIPTION - The first substrate(10) is provided with the window(14) for exposing the first groove(12). The first semiconductor chip of center pad type is attached to expose a bonding pad through the first window. The second substrate(20) with the second widow(24) for exposing the second groove(22) is attached on the first substrate to expose edge portions of the first substrate.

The second semiconductor chip is attached in the second groove of the second substrate. A plurality of bonding wires(30,32) are connected between the first electrode terminals(16a,16b) of the first substrate and the second electrode terminals(26a,26b) of the second substrate. Solder balls(40) are attached at a back side of the first substrate.

CHOSEN-DRAWING: Dwg.1/10

TITLE-TERMS: CHIP STACK PACKAGE

DERWENT-CLASS: U11

EPI-CODES: U11-D01A6; U11-E01A; U11-E02A3;